Remarks:

In the Office Action mailed on November 26, 2007, the Examiner rejected claims 1-39.

Applicants amend claims 1, 2, 4, 9, 11, 12, 13, 23, 25 and 30 herein. Claims 40 and 41 are added herein.

Claims 1-41 are pending in the application.

The Claims

35 USC 102

Claims 1-2, 11, 13, 23, 32-35 and 38-39 were rejected under 35 U.S.C. 102(b) as being anticipated by Ban (WO/94/20906 hereinafter Ban).

Anticipation under 35 U.S.C. 102(b) requires that each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference", *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1

While Ban, like applicant, addresses writing into a flash memory, Ban's approach is quite different from the method described and claimed by applicants.

In a flash type memory data is written by merely turning bits having the value zero to the value one. That, of course, only works if the

bits that are to be zero after the write were already zero before the write. Otherwise, the data location has to first be erased. Thus, writes normally involves zeroing out the data location and then writing the required one bits. Applicants address the issue that erasing a flash memory is a very costly operation in contrast to write operations. Thus, when an operation is performed that requires an erase operation, that operation is costly.

Applicant's solution is to associate a plurality of physical areas of the memory to each logical area. Figure 2 of the present application provides an illustration of this arrangement. Each logical area ZL has a plurality of physical areas ZPi associated therewith. One such area is designated as the active area. When a write operation is made to the logical area ZL, that write operation translates into a write operation on *the* active physical area. Write operations that require clearing of bits may be performed by rather than writing into the current active physical area, a new active physical area, one that has previously not been written to, is designated. Erase operations can be made when convenient, e.g., during idle moments. Thus, the write operations are generally optimized.

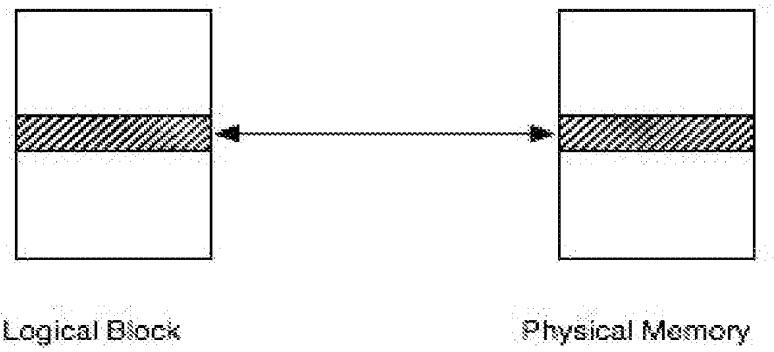
In his response to arguments section, the Examiner stated that the argued stationary association between the physical areas to a same and unique logical area is not recited in the claims. Office Action, Page 24, Lines 4-7. Applicants have amended the claims to more clearly recite the subject matter of the invention. Of note, Applicants now clearly indicate that each physical area is designated to correspond to a same logical area.

Applicants thus claim, "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" (Claim 1). One of the areas is "designat[ed] … as being an active physical area", and "during a write to said logical area, programming the content of said logical are into the active physical area." (Claim 1).

Ban's solution does not teach or suggest these steps.

Ban fails to teach or suggest "at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" (Claim 1). In Ban, Fig. 4, element 35, "a logical unit table 35 translates *the* logical unit number to *a* physical unit number for *the* logical unit" (Ban, page 8, lines 8-9) and "the logical address is mapped to *a* physical address in the flash memory" (page 8, lines 22-23). Thus, it is clear that there is a one-to-one mapping in Ban between logical units and physical units. Nowhere does Ban say anything to the contrary.

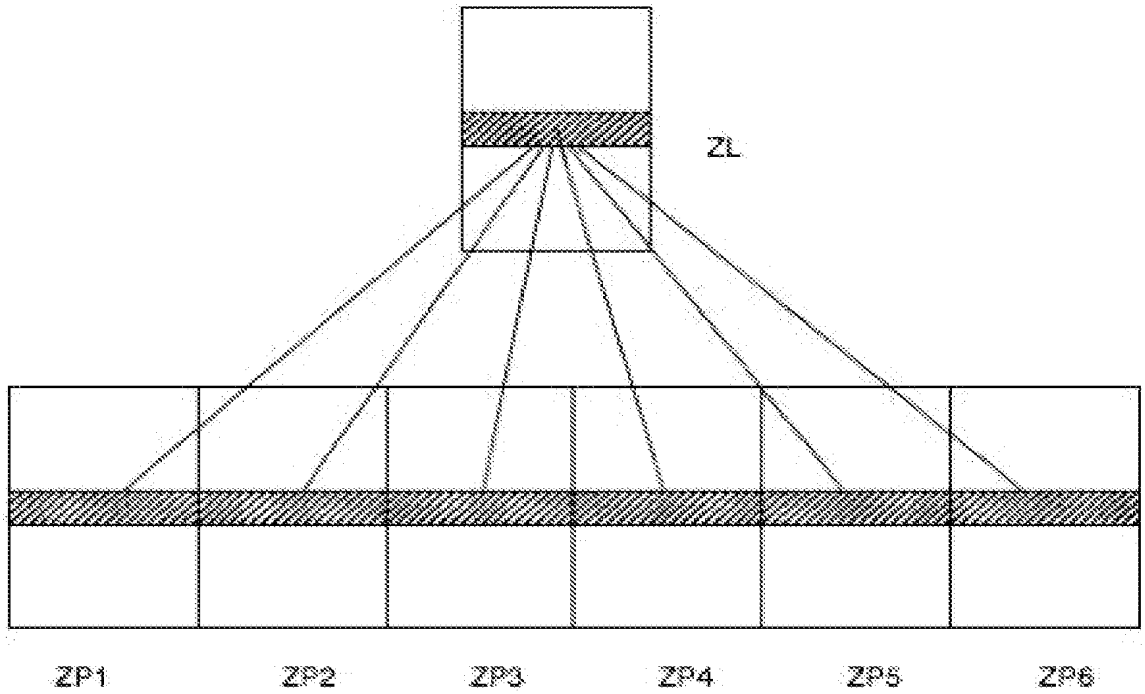
The mapping in Ban between addresses in the logical block address space and the physical memory is illustrated below:[1]



For a particular addressable entity (e.g., a byte) in a logical block is mapped to a corresponding address in the physical memory. The two shaded areas represent such mapped addressable entities. Thus, of course, a given logical block will be mapped to many physical memory locations, precisely one for each of its addressable locations.

Applying that aspect of Ban's teaching to the present application, each physical area in the mirror area would have the same correspondence as the one-to-one mapping between logical block addresses and corresponding physical areas in the mirror area. That is illustrated below:

[1] In fairness to Ban, much of that reference deals with how that mapping between virtual address space, logical units, and physical memory. Figure



For each physical block there is a corresponding address.

From the foregoing illustrations it must be clear that Ban's teaching is not equivalent to "at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" and that the Examiner's reading of Ban's physical addresses corresponding to logical block addresses as being equivalent is not correct.

While Ban organizes the memory into blocks and units, in writing to a unit, if a logical address is not free, an available free address is located. Ban, Page 9, lines 14-15. To reclaim memory, periodically all active blocks of one unit are copied into another unit, the TRANSFER unit, and the originating unit is flash erased. Ban, page 9, lines 23-26. However, there is no association of multiple physical areas of memory to a particular logical area as is claimed herein. Ban does not disclose or suggest a stationary association of a group of physical areas to a same and unique logical area.

An advantage of Applicants' claimed invention in comparison to Ban is that in Applicants' solution there is not a need for Ban's mechanism

for releasing physical areas for use by other logical areas. Further, because each logical area would have at least two physical areas associated therewith, Applicants' memory would be faster than a memory with dynamic allocation of physical areas such as proposed by Ban.

In the response to arguments section, the Examiner indicated disagreement with Applicant in regards to Ban teaching a one-to-one mapping. The Examiner pointed to Ban's statement that "Here it should be noted, the virtual address space is not necessarily the same size as the physical address space. (Page 2, lines 26-28)." (Office Action, Page 24). Applicants disagree that that statement contradicts Applicants' position vis-à-vis Ban.

Typically virtual addressing is used precisely to deal with limits in a physical address space. Many addressing schemes allow for addressing much larger spaces than the available physical space. Mapping virtual addresses to physical addresses in a clever way addresses that mismatch between the addressing capabilities of a machine versus the actual available physical space.

That makes sense in the context of Ban as well. Ban goes on to say that "[associated] in the table with each virtual block address there is a corresponding physical address." (Ban, Page 3, Lines 9-11). Thus, for each virtual block there is one physical block. In a virtual addressing scheme, the virtual space can be larger than the physical area available. Therefore, for each virtual address used there needs to be a mapping to a physical area. Implicit is that there cannot be more virtual space in active use than there is physical space available because if there were, more space would be in use than is available.

While there can be a difference in the virtual space and the physical space, there is no indication that multiple physical address blocks are used for the same virtual address block. That is not surprising because Ban's system operates on a different principle.

The Examiner states "it can be reasonably interpreted that the physical units can be the physical byte addresses from the physical block, and the logical/virtual block corresponds to 512 byte physical block (address with denotes a 512 byte range, ie. beginning address + offset = physical block address) or 512 single physical byte addresses (page 3, lines 1-29)" (Office Action, Paragraph bridging pages 24-25). That statement only shows that a logical block that spans more than one address will have multiple physical addresses. However, any given address in the logical block only maps to one physical address and conversely the logical block itself only maps to one physical area.

Ban's of dealing with writing to physical areas that cannot be written to is also telling. As with all flash memories, Ban must address what to do when encountering a block that cannot be written to. Ban describes that when writing to a physical block that cannot be written to, "an unwritten block is therefore located and written to. The virtual memory map is changed so that the unwritten physical block is mapped to the original virtual address and original physical block is denoted as unusable." (Ban, Page 3, Lines 19-24). Thus, Ban's method for dealing with writing to physical blocks that have already been written is to find a new block and to manage this block-allocation through a memory map. That is a clear indication that Ban does not teach or suggest "at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" because using the mirror areas as claimed herein, such remapping in a virtual memory map is not necessary.

Therefore it is not surprising that Ban's way of dealing with the problem of writing to a physical area that cannot be written to does not teach or suggest Applicants' claim that "a mirror area in the flash type memory [is] divided into at least two physical areas ... each designated to correspond to a same logical area." Implicit in this claim is an association

between the at least two physical areas and the logical area. That is in clear contradistinction to Ban where there is an explicit one-to-one mapping between virtual areas, logical areas, and physical areas (see Figure 4) and a dynamic allocation of new areas when there is a need to write to an already written-to physical block.

Accordingly, Applicants respectfully submit that Ban fails to teach or suggest, "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" as required by claim 1 and therefore claim 1 is not anticipated by Ban and is patentable over Ban.

Claims 11 and 13

Claim 11 and 13 recite analogous limitations and should be allowed for, at least, the same reasons given in support of Claim 1.

Claims 2, 23, 32-35 and 38-39

Claims 2, 23, 32-35 and 38-39 are all dependent claims deriving from the independent claims, incorporating the limitations of the independent claims, provide further unique and non-obvious combinations, and are therefore patentable over Ban for, at least, the reasons given in support of the independent claims and by virtue of such further combinations.

35 USC 103

Claims 3, 7-8, 18, 24 and 28-29 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban (WO/94/20906, hereinafter Ban) as applied to claims 1-2, 13 and 23 above and in further view of Assar et al (WO 95/10083 hereinafter Assar). Claims 4 and 25 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1 and 13 and

further in view of Mennecart (WO 01/88926 A1) hereinafter Mennecart. Claims 5 and 26 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 2 and 13 and further in view of Hazen et al (WO 99/35650) hereinafter Hazen. Claims 6 and 27 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 26 and in view of Lipovski (US 5,758,148) hereinafter Lipovski. Claims 9-10 and 30-31 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban as applied to claims 1-2 and 13 and further in view of Kuo (US 4,763,305) hereinafter Kuo. Claims 12, 36 and 37 are rejected under 35 U.S.C.103 (a) as unpatentable over Ban and further in view of Robinson et al (US 5,375,222). Claims 14-17 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claims 5 and 6 and further in view of Assar. Claims 19-20 were rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Hazen as applied to claim 5 and 6 and further in view of Kuo. Claims 21-22 is rejected under 35 U.S.C.103 (a) as unpatentable over Ban in view of Assar as applied to claim 7 and further in view of Kuo.

Ban

As discussed hereinabove with respect to the 35 USC 102 rejections, Claim 1, 11, 12, and 13 are patentable over Ban.

Assar, Mennecart, Hazen, Lipovski, and Kuo are cited by the Examiner for propositions other than those argued hereinabove. None of these references teach or suggest "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area; designating one of the physical areas as being an active physical area; and during a write to said logical area programming the content of said logical area into the active physical area" (Claim 1 and analogous in

the other independent claims). Therefore, Claim 1 and the other independent claims are patentable over these references taken singly, or in any combination including or not including Ban.

Therefore, because all the dependent claims depend from the independent claims, incorporate all the limitations thereof and provide further unique and non-obvious combinations, the dependent claims are patentable for, at least, the reasons given in support of the independent claims.

Claim 9, 30, 40, and 41 all deal with writing to a logical area when the active physical area cannot be written to. Claim 9 recites "if the content of the logical area is identical to the content of the active physical area or when said write involves no erasure, the write is carried out in an active physical area and in a blank physical area in the mirror area otherwise" (and similarly in Claim 30). Claim 40 recites "determining whether writing to the active physical area would require an erase operation prior to writing; in response to determining that writing to the active physical area would require an erase operation, designating an unwritten physical area in the mirror area as the active physical area; and storing an indication that the active physical area is a written memory area" (similarly in 41). Because Ban (and the other references) does not teach or suggest "defining a mirror area in the flash type memory divided into at least two physical areas each designated to correspond to a same logical area for storing content written to the logical area" it is not surprising that Ban does not teach or suggest allocating a blank physical area in the mirror area" (Claim 9, similar in Claim 30, 40, and 41). Accordingly, these claims are patentable over Ban (and the other reference taken singly or in combination) for this additional reason.

The application is now deemed to be in condition for allowance and notice to that effect is solicited.

CONCLUSION

It is submitted that all of the claims now in the application are allowable. Applicants respectfully request consideration of the application and claims and its early allowance. If the Examiner believes that the prosecution of the application would be facilitated by a telephonic interview, Applicants invite the Examiner to contact the undersigned at the number given below.

Applicants respectfully request that a timely Notice of Allowance be issued in this application.

Respectfully submitted,

Date: January 9, 2009

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